FE1.1s

USB 2.0 High Speed 4-Port Hub Controller

Product Brief

Introduction

The FE1.1s is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 High Speed 4-Port Hub.

It adopts *Single Transaction Translator* (STT) architecture to be more cost effective. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special *Build-In-Self-Test* mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stage as well.

Low power consumption is achieved by using 0.18 μm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

Features

- Low power consumption
  - 100 mA when four Downstream ports enabled in High-Speed mode;
  - 57 mA when one Downstream port enabled in High-Speed mode;
- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Single Transaction Translators* (STT) –
  - One TT for all downstream port;
  - The TT could handle 64 periodic Start-

Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;

- Automatic self-power status monitoring;
  - Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- *Ganged Power Control* and *Global Over-Current Detection* support;
- EEPROM configured options –
  - *Vendor ID*, *Product ID*, & *Device Release Number*; and
  - *Number of Downstream Ports*;
- Comprehensive Port Indicators support:
  - *Downstream Port Enabled* indicator LED (x4, Green);
  - Hub Active/Suspend indicator LED;
- Support Microsoft Windows 98SE/ME, 2000, XP, and Vista;
- Support Mac OS 8.6 and above;
- Support Linux kernel 2.4.20 and above.

PACKAGE

28-pin SSOP
(Body Size: 10x4 mm; Pitch: 0.64 mm)

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