The FE1.1 is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 4-Port Hub.

It adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by Test Scan Chain – include even the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise all high, full, and low speed analog components on the packaging and testing stage as well.

Low power consumption is achieved by using 0.18 μm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

FEATURES

- Low power consumption
  - 115 mA when four Downstream ports enabled in High-Speed mode;
  - 64 mA when one Downstream port enabled in High-Speed mode;
- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resistors;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- Multiple Transaction Translators (MTT) –
  - One TT for each downstream port;
  - Alternate Interface 0 for Single-TT, and
Alternate Interface 1 for Multiple-TT;
- Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- Automatic self-power status monitoring;
- Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- Board configured options –
  - Ganged or Individual Power Control Mode select;
  - Global or Individual Over-Current Detection Mode select;
  - Removable or Non-Removable Downstream Devices configuration;
- Comprehensive Port Indicators support:
  - Standard downstream port status indicators (Green and Amber LED control for each downstream port);
  - Hub active LED support;
- Support Microsoft Windows 98SE/ME, 2000, XP, and Vista;
- Support Mac OS 8.6 and above;
- Support Linux kernel 2.4.20 and above.

**PACKAGE**

48-pin LQFP (Body Size: 7x7 mm)
48-pin QFN (Body Size: 6x6 mm, 0.4 pitch)